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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/812,177
Filing Date: March 29, 2004
Appellant(s): INOUE, KEISUKE

Andrew T. Zidel
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 30 June 2008 appealing from the Office action mailed 4 February 2008.

(1) Real Party in Interest

A statement identifying by name the real part in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of the claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The Appellants statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief are correct.

(8) Evidence Relied Upon

(8.1) Chauvel et al. "Temperature Field Controlled Scheduling for Processing Systems", U.S. Patent Application No. 2002/0065049.

(9) Grounds of Rejection

The following grounds of rejection are applicable to the appealed claims:

(9.1) Claims 1-11, 24, 26-31, 33-34, 53-60, and 63 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

i) Claim 1 recites providing, associating, and scheduling operations. Therefore the claim does not produce a useful, concrete, and tangible result. The resultant of the claims is neither stored, nor provided to a user,

etc., for example, and therefore does not contain a concrete and tangible result.

ii) Claim 24 recites a computing device with a plurality of associated operations. The association of operations appears to be mere data manipulation and therefore the claims do not produce a useful, concrete, and tangible result.

iii) With respect to claims 1-12, 24-34, and 53-63, paragraph 74 of the instant application recites, "The compiler may be implemented in software, firmware, hardware or a combination of the above." Therefore the claimed limitations may be entirely software and are therefore non-statutory since "software per se" does not fall under an approved statutory category.

Appropriate correction is required.

All claims dependent upon a rejected base claim are rejected by virtue of their dependency.

(**9.2**) **Claims 1-11, 13-24, 26-31, 33-60, and 63-89 are rejected** under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

i) Claims 1-11, 13-24, 26-31, 33-60, and 63-89 are rejected by virtue of undue multiplicity. Section 2173.05(n) of the MPEP states ***"37 CFR 1.75. Claim(s). (a) The specification must conclude with a claim particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention or discovery. (b) More than one claim may be presented provided they differ substantially from each other and are not unduly multiplied. Where, in view of the nature and scope of applicant's invention, applicant presents an unreasonable number of claims which are repetitious and multiplied, the net result of which is to confuse rather than to clarify, a rejection on undue multiplicity based on 35 U.S.C. 112, second paragraph, may be appropriate. As noted by the court in In re Chandler, 319 F.2d 211, 225, 138 USPQ 138, 148 (CCPA 1963), "applicants should be allowed reasonable latitude in stating their claims in regard to number and phraseology employed. The right of applicants to freedom of choice in selecting phraseology which truly points out and defines their inventions should not be abridged. Such latitude, however, should not be extended to sanction that degree of repetition and multiplicity which beclouds definition in a maze of confusion. The rule of reason should be practiced and applied on the basis of the relevant facts and circumstances in each individual case." See also In re Flint, 411 F.2d 1353,***

1357, 162 USPQ 228, 231 (CCPA 1969)."

The now 84 claims and 11 independent claims contain limitations from multiple embodiments that are assorted into multiple different independent claims in an unclear manner and result in a "maze of confusion." The Examiner contacted Applicants representative, Andrew Zidel, Reg No. 45,256, to allow Applicants the opportunity to provide a preliminary amendment to resolve the undue multiplicity. Applicants representative elected claims 1-12, 24-34, and 53-63 to be examined. All claims dependent upon a rejected base claim are rejected by virtue of their dependency.

(9.3) Claims 1-11, 24, 26-31, 33-34, 53-60, and 63 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by **Chauvel et al. "Temperature Field Controlled Scheduling for Processing Systems", U.S. Patent Application No. 2002/0065049.**

Regarding Claim 1:

The reference discloses A method of scheduling operations to be performed by a component having a thermal threshold comprising:

providing a plurality of operations to be performed by the component; **(Abstract. Figure 11. Paragraph 52)**

associating the operations with a thermal attribute, the thermal attribute representing a value related to a heat amount expected to be generated or incurred by the component during performance of the operations; **(Abstract. Figure 11. Paragraph 52)**

determining a cooling attribute; **(Paragraph 8)**

and scheduling the operations in an order of performance based on the thermal attribute and the cooling attribute so that the thermal threshold is not exceeded. **(Abstract. Figure 11. Paragraph 52)**

generating the order of performance for use in execution of the operations. **(Paragraph 49)**

Regarding Claim 2:

The reference discloses The method of claim 1, further comprising measuring the thermal attribute with a temperature sensing means. **(Paragraph 53, Temperature Measurement)**

Regarding Claim 3:

The reference discloses The method of claim 1, further comprising estimating the thermal attribute based upon power consumption of the component. **(Paragraph 3)**

Regarding Claim 4:

The reference discloses The method of claim 3, wherein estimating the thermal attribute further includes performing a circuit simulation of the component. **(Paragraph 35, "experimentally or by computer aided software design.")**

Regarding Claim 5:

The reference discloses The method of claim 3, wherein estimating the thermal attribute further includes determining a power density of the component. **(Paragraph 29, "power management tasks")**

Regarding Claim 6:

The reference discloses The method of claim 1, further comprising the component executing the operations in the order of performance. **(Paragraph 32)**

Regarding Claim 7:

The reference discloses The method of claim 6, wherein the component includes a plurality of processing devices and the thermal attribute is an aggregate thermal attribute of selected ones of the processing devices that execute the operations. **(Claim 1)**

Regarding Claim 8:

The reference discloses The method of claim 1, wherein the component includes a plurality of processing devices, each of the processing devices has an individual thermal threshold, and the thermal attribute includes a plurality of individual thermal attributes, each individual thermal attribute being associated with one of the processing devices. **(Claim 1)**

Regarding Claim 9:

The reference discloses The method of claim 8, further comprising:

selecting at least some of the processing devices to execute the operations; **(Figure 3a-3b. Paragraph 34-35)**

monitoring the selected processing devices; **(Figure 3a-3b. Paragraph 34-35)**

and routing the operations among the selected processing devices so that the individual thermal thresholds are not exceeded. **(Figure 3a-3b. Paragraph 34-35)**

Regarding Claim 10:

The reference discloses The method of claim 1, wherein the component includes a plurality of processing devices and the thermal attribute is allocated among the plurality of processing devices. **(Figure 3a-3b. Paragraph 34-35)**

Regarding Claim 11:

The reference discloses The method of claim 1, further comprising determining the thermal attribute by:

(i) determining power consumption of the component; **(Figure 3a-3b. Paragraph 34-35)**

(ii) determining a footprint of the component; **(Figure 3a-3b. Paragraph 34-35)**

(iii) dividing the power consumption of the component by the footprint of the component to obtain per-area power consumption; **(Paragraph 12, 49)**

and (iv) multiplying the per-area power consumption by a thermal estimation constant. **(Paragraph 12, 49)**

Regarding Claim 24:

The reference discloses A processing system comprising:

a computing device including a component; **(Abstract. Figure 11. Paragraph 52)**

a plurality of operations to be performed by the component, at least some of the operations including a priority; **(Abstract. Figure 11. Paragraph 52)**

and at least one thermal attribute associated with the component and a selected one of the operations, the thermal attribute being indicative of a change in temperature of the component after performance of the selected operation. **(Abstract. Figure 11. Paragraph 52)**

a plurality of priority queues, each priority queue including a first queue and a second queue, the first queue for storing a first set of the operations and the second queue for storing a second set of the operations; **(Paragraph 49)** and

a scheduler operable to assign at least one of the operations to the component depending on the thermal attribute. **(Paragraph 49)**

Regarding Claim 26:

The reference discloses The processing system of claim 24, wherein the scheduler is operable to retrieve a chosen one of the operations from a storage location depending upon the thermal attribute. **(Abstract. Figure 11. Paragraph 52)**

Regarding Claim 27:

The reference discloses The processing system of claim 24, wherein the component includes a plurality of sub-components, the scheduler is a simple scheduler, and the thermal attribute is a total thermal attribute associated with the component and not associated with the plurality of sub-components. **(Paragraph 9, 51)**

Regarding Claim 28:

The reference discloses The processing system of claim 24, wherein the component includes a plurality of sub-components, the scheduler is an advanced scheduler, and the thermal attribute is further associated with at least some of the sub-components. **(Paragraph 12, 49)**

Regarding Claim 29:

The reference discloses The processing system of claim 24, wherein the component is a processing device and the scheduler is integrated with the processing device. **(Abstract. Figure 11. Paragraph 52)**

Regarding Claim 30:

The reference discloses The processing system of claim 24, wherein the selected operation comprises a task, and the thermal attribute is a task thermal attribute. **(Abstract. Figure 11. Paragraph 52)**

Regarding Claim 31:

The reference discloses The processing system of claim 24, wherein the task thermal attribute is based on at least one of an operating frequency of the component, a thermal attribute of the component, and a cooling attribute. **(Paragraph 8, 39)**

Regarding Claim 33:

The reference discloses The processing system of claim 24, further comprising a scheduler operable to assign at least some of the operations to either the first or the second queue in a selected one of the priority queues based on the priorities of the operations and on the thermal attribute. **(Paragraph 30)**

Regarding Claim 34:

The reference discloses The processing system of claim 33, wherein the scheduler is further operable to retrieve a chosen one of the operations from the first queue or the second queue of the selected priority queue depending upon the thermal attribute and the priority of the chosen operation. **(Paragraph 30)**

Regarding Claim 53:

The reference discloses A processing apparatus for processing operations associated with thermal attributes, comprising:

a memory for storing a first operation and a second operation, the first operation having a thermal attribute exceeding an operating threshold, and the second operation having a thermal attribute not exceeding the operating threshold; **(Abstract. Figure 11. Paragraph 52)**

and a plurality of processing devices for executing the first and second operations, at least a selected one of the processing devices comprising a sub-processing unit, and at least some of the processing devices having a thermal threshold and access to the memory; **(Abstract. Figure 11. Paragraph 52)**

wherein, if the thermal threshold of the selected processing device is not exceeded, the selected processing device is operable to obtain the first operation from the memory for processing and to process the first operation, **(Abstract. Figure 11. Paragraph 52)**

and if the thermal threshold of the selected processing device is exceeded, the selected processing device is operable to obtain the second operation from the memory for processing and to process the second operation, and **(Abstract. Figure 11. Paragraph 52)**

wherein the memory comprises a local store in the sub-processing unit, and the local store includes a first queue for managing the first operation and a second queue for managing the second operation. **(Paragraph 49)**

Regarding Claim 54:

The reference discloses The processing apparatus of claim 53, wherein at least some of the processing devices are processing elements. **(Figure 3a-3b. Paragraph 34-35)**

Regarding Claim 55:

The reference discloses The processing apparatus of claim 54, wherein at least some of the processing elements further comprise at least one sub-processing unit. **(Figure 3a-3b. Paragraph 34-35)**

Regarding Claim 56:

The reference discloses The processing apparatus of claim 55, wherein each sub-processing unit includes a floating point unit, an integer unit and a register associated with the floating point unit and the integer unit. **(Figure 3a-3b. Paragraph 34-35)**

Regarding Claim 57:

The reference discloses The processing apparatus of claim 56, wherein each sub-processing unit further includes a local store. **(Figure 3a-3b. Paragraph 34-35)**

Regarding Claim 58:

The reference discloses The processing apparatus of claim 54, wherein at least some of the processing elements further comprise a processing unit and a plurality of sub-processing units associated with the processing unit. **(Figure 3a-3b. Paragraph 34-35)**

Regarding Claim 59:

The reference discloses The processing apparatus of claim 58, wherein the sub-processing units each further include a local store. **(Figure 3a-3b. Paragraph 34-35)**

Regarding Claim 60:

The reference discloses The processing apparatus of claim 53, wherein a first one of the processing devices is operable to exchange operations with a second one of the processing devices depending upon the thermal threshold of the first processing device. **(Figure 3a-3b. Paragraph 34-35)**

Regarding Claim 63:

The reference discloses The processing device of claim 53, wherein the first and second operations are maintained in the memory in a timesharing arrangement. **(Paragraph 30)**

(10) Response to Argument

Response to Argument – Non-Prior Art Rejections

(10.1) Appellant argues the 112 2nd rejections of the claims with respect to undue multiplicity.

Examiners Answer:

The Examiner notes that Appellents arguments fully support the reasoning behind the Examiners rejection. First, Appellants devote pages 18-20 of their Appeal Brief for explanation as the content of independent method claims 1, 13, 44, 50, and 66, system claims 24, 35, and 76, apparatus claims 53, 64, and 65. Just based on the explanations of the claims provided it can be seen that the multitude of independent claims result in "maze of confusion." The eleven independent claims intersperse limitations regarding thermal attributes, thermal thresholds, scheduling, priority, and tasks. However it is unclear how the claims inter-relate to each other for the purposes of patent coverage or furthermore how they serve to clarify Appellants invention. For example:

Claim 1 recites thermal attributes, thermal thresholds, and scheduling.

Claim 13 recites thermal attributes, thermal thresholds, and scheduling.

Claim 24 recites thermal attributes, priority, and scheduling.

Claim 35 recites thermal attributes, thermal thresholds and scheduling.

Claim 44 recite thermal attributes and thresholds.

Claim 50 recites thermal thresholds.

Claim 53 recites thermal atributes, thermal threshold, subprocessing, and scheduling.

Claim 64 recites thermal attributes and thresholds, and subprocessing.

Claim 65 recites thermal attributes and thresholds, and subprocessing.

Claim 66 recites thermal attributes and tasks.

Claim 76 recites thermal attributes and tasks.

Merely based on the simplified explanation of the claims it is clear that the 11 independent claims assorting at least half a dozen different variations of another half a dozen claim limitations is confusing and counterproductive to the clarity of the application and the invention. The issue is not merely the large number of independent claims but also the lack of any coherent connection between them or even an explanation by Appellants as to how the claims are related and how they represent different potential embodiments. Appellants have maintained arguments disputing the validity of the rejection without attempting to merely explain the rationale behind the combination of the claims in order to overcome the confusion they present. Finally, the Examiner contacted Appellants representative, Andrew Zidel, Reg No. 45,256, to allow Appellants the opportunity to provide a preliminary amendment to resolve the undue multiplicity. Instead, Appellants elected claims 1-12, 24-34, and 53-63 to be

examined which is how the Examiner proceeded. The Examiner notes that Applicants did not disagree with the reasoning provided or the rejection itself when they elected claims 1-12, 24-34, and 53-63 to be examined.

Response to Argument – Non-Prior Art Rejections

(10.2) Appellant argues the 101 rejections of the claims.

Examiners Answer:

Claim 1 recites providing, associating, and scheduling operations. The resultant of the claims is neither stored, nor provided to a user, etc., for example, and therefore does not contain a concrete and tangible result. Moreover the claims appear to amount to a manipulation of data. The generating an order of performance, scheduler, and obtaining an operation from memory do not represent tangible results. These limitations appear to be mere data manipulation and as such are non-statutory.

Claim 24 recites a computing device with a plurality of associated operations. The association of operations appears to be mere data manipulation and therefore the claims do not produce a useful, concrete, and tangible result.

With respect to claims 1-12, 24-34, and 53-63, paragraph 74 of the instant application recites, "The compiler may be implemented in software, firmware, hardware or a combination of the above." Therefore the claimed limitations may be entirely software and are therefore non-statutory since "software per se" does not fall under an approved statutory category. As per the specification of the instant application the compiler is associated with the processing devices and components, see paragraph 76 of the instant application, and therefore since the claims recite these elements and a compiler is associated with these elements the 101 rejections are maintained. The claims are not being limited by the citation of the specification provided by the Examiner. The Examiner is merely pointing out that the compiler can encompass software **(See Page 26 of Appeal Brief, paragraph 3 which states one aspect of the invention "may include a compiler"),** and the claims need not explicitly recite the compiler since as per the specification the compiler is a clear part of the processing devices and components which are explicitly recited in the claims. The Examiner notes that the compiler is a key part of Applicants invention, as can be seen in Figures 2 and 11.

Appellants further argue, with respect to claim 6 the order of execution of components is not abstract, with respect to claim 9 routing operations, and with respect to claim 24 a computing device render the claims statutory. The order of execution of components and routing operations represent mere abstract software elements with no correlation to a tangible result or physical transformation. Further the addition of a computing device does not obviate the non-statutory nature of the claims since it is Office policy that the mere recitation of a physical device does not necessarily result in a physical transformation. See Gottschalk v. Benson, 409 U.S. 63, 71-72, 175 USPQ 673, 676 (1972).

Response to Argument – Prior Art Rejections

(10.3) Appellant argues that the reference does not teach a cooling attribute. (ARGUMENT A on pages 37-39 of Appeal Brief)

Examiners Answer:

Appellants argue that Chauvel does not teach a "cooling attribute." Appellants further argue that the broadest reasonable interpretation of a cooling attribute should be defined in view of Applicants specification. First, as noted by Appellants on the top of Page 22 of their remarks dated 5 November 2007, **"it is black letter law that it is improper to read limitations from the specification into the claims." (Emphasis added).** In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e.,"cooling attribute" as allegedly defined in Appellants specification) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The Examiner also notes that the term "cooling attribute" is mentioned in the speciation in for example paragraphs 14, 20, and 23 but no explicit definition is provided.

Therefore the Examiner once again takes the broadest reasonable definition of the term "cooling attribute" which the Examiner contends is discussed in the reference in a plurality of ways. First, the reference discusses "temperature associated information", see paragraph 11 of Chauvel, as well as temperature thresholds as per paragraph 12 of Chauvel, as well as temperature effects, see paragraph 52 of Chauvel. Further, the inherent nature of

heat as it relates to IC's (integrated circuits) is that following a drop in power provided to an IC the temperature will drop. Second, the references discussion of the dissipation of heat reads on a cooling attribute, see at least paragraph 8 of Chauvel. Further, cooling mechanisms and attributes are inherent in the desktop/portable computers discussed in the reference in the form of fans and heat sinks as well as in the inherent nature of cooling in that following a lack of power supplied to an IC the IC will begin to cool. Finally the Examiner notes that the definition of cooling is the absence or dissipation of heat since cold is measured by a lack of heat not by a measure of amount of cold. This is a principal parameter of thermodynamics.

Response to Argument – Prior Art Rejections

(10.4) Appellant argues that the reference does not teach a queue or dual queue configuration. (ARGUMENT B on pages 39-41 of Appeal Brief)

Examiners Answer:

Appellants argue that a **"queue"** is not **"merely a schedule of tasks"** as asserted in the previous rejection. As per Appellants specification a queue is exemplary defined, not explicitly, as a "set of operations" **(See Paragraph 24 of the specification of the instant application).** First, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e.,"queue" as defined in Applicants specification) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Applicants also argue that Chauvel does not teach a dual queue configuration.

Based on the broadest reasonable definition of the term "queue", as a "set of operations" or a "schedule of tasks", Chauvel in paragraph 49, discusses task rescheduling for multiple processors, MPU/DSP, based on priority. Multiple processors as well as utilizing energy consumption as a criterion for scheduling of multiple tasks in the multiple processors can be seen at the end of paragraph 30 as well paragraph 31 of Chauvel. This anticipates multiple queues which therefore anticipates a dual queue. **This further applies to (ARGUMENT D on pages 42-44 of Appeal Brief)**

The Examiner notes that Appellants argue that the Examiner cited particular sections of the prior art without explanation. The Examiner contends that any and all issues raised by Appellants were directly and explicitly responded to in the previous office actions. For example, Appellants state that the Examiner cited paragraph 49 with no explanation however the arguments presented above were presented in the previous office action.

Response to Argument – Prior Art Rejections

(10.5) Appellant argues that the reference does not teach the limitations of claim 31. (ARGUMENT C on pages 41-42 of Appeal Brief)

Examiners Answer:

Appellants argue that Chauvel does not teach a task thermal attribute is based on at least one of an operating frequency of the component, a thermal attribute of the component, and a cooling attribute. The Examiner cites the heat dissipation in paragraph 8 of Chauvel which reads on a thermal attribute and a cooling attribute. A cooling attribute is equivalent to a thermal attribute since as mentioned above the measure of cold is done by measuring the amount of heat.

Response to Argument – Prior Art Rejections

(10.6) Appellant argues that the reference does not teach the limitations of claim 63, specifically the time sharing arrangements. (ARGUMENT E on page 44 of Appeal Brief)

Examiners Answer:

The recitation in Paragraph 30 of Chauvel is with respect to multiprocessor systems which execute multiple tasks through scheduling. It is an inherent aspect of multiprocessor systems to execute multiple tasks at the same time. This anticipates the time sharing of a first and second operation recited in claim 63.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the Examiner in the Related Appeals and Interferences section of this Examiner's Answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Saif Alhija, Patent Examiner

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